ABSTRACT

The present invention aims at providing a photodetector which can secure both a good S/N ratio and a high speed. With a photodetector 1, (K × M × N) photodiodes $PD_{k,m,n}$ are arranged in M rows and (K × N) columns in a photodetection unit 10, and processes (electric charge accumulation, CDS, filtering, and A/D conversion) regarding each of the (K × N) photodiodes $PD_{k,m,n}$ (k = 1 to K, n = 1 to N) of each row are carried out successively at each time T. Meanwhile, each of an electric charge accumulation operation in an integrating circuit $20_{m,n}$, a CDS operation in a CDS circuit $30_{m,n}$, a filtering operation in a filter circuit $40_{m,n}$, and an A/D conversion operation in an A/D converter $50_{m,n}$ is carried out at each time (N × T).